REMARKS

Reconsideration and further examination are respectfully requested. Claims 1-18 are currently pending.

Rejections under 35 U.S.C. §103

Claims 1 and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Davis et al. (U.S. Patent 5,377,617) , in view of "The RISC Concept – A survery of Implementations", Esponda et al., (hereinafter Esponda), September 1991.

Davis:

Davis describes, in the Abstract:

"... hybrid pipelined processor and associated processing methods ... for separately handling substantially concurrently in a time division manner multiple program instruction threads. The hybrid architecture includes an instruction fetch unit, an instruction decode unit and an execution unit. The execution unit includes multiple sets of register files each of which contains the working contents for a corresponding one of a plurality n of instruction threads. Timing and control circuitry is coupled to each of the principal processor components for controlling the timing and sequence of operations on instructions from the plurality n of instruction threads such that multiple instruction threads are separately handled substantially concurrently...."

Esponda

Esponda describes the basic concepts of the Reduced Instruction Set Computer (RISC) architectures. Esponda states, at page 5, lines 5-11:

"... In real systems there are many reasons for the regular pipeline flow to be interrupted systematically. The penalty for these disruptions is paid in the form of lost or stall pipeline cycles. The effective parallelism exploited by traditional CISC microprocessors .... is rarely larger than the factor 2, and more likely to be near the factor 1.5. This means that old CISC microprocessors offer very limited form of pipeline parallelism...The main different between RISC and CISC is that the instruction set of the first kind of processors was explicitly designed to allow the sustained execution of instructions in one cycle as average..."

The Examiner states, at pages 4-5 of the office action:

"... Munson does not explicitly teach: executing the first instruction in a first stage of a processing pipeline... and forwarding the first instruction to a next stage of the processing pipeline while forwarding the second instruction to the first stage of the processing pipeline such that the first instruction and the second instruction can be executed simultaneously in the processing pipeline...However, Esponda teaches executing a first instruction in a first stage of a processing pipeline .... first instruction being *instruction i,* and first stage being *instruction fetch,*) and forwarding the first instruction to a next stage of the processing while forwarding the second instruction to the first stage of the processing pipeline such that the first instruction and second instruction can be executed simultaneously in the processing pipeline... It would have been obvious to a person of ordinary skill in the art ... to combine the teachings of Munson and Esponda because teaching of Esponda include multiple stages within a pipeline achieving parallel execution of instruction threads would improve the efficiency of Munson by allowing for execution of instruction by a factor of three (Esponda, pg. 5, lines 1-5)..."

Combination neither describes nor suggests the claimed invention

Both Esponda and Davis deal with sequential instructions in a stream. Applicants have amended the claims to clarify that the present invention is concerned with multi-packet threads. Thus, in contrast to an instruction being prosecuted at each pipeline stage, a packet is processed. As described on page 5 of Applicants' invention, one advantage of such an architecture that is not shown or suggested by the art is that the multi-thread packet processor may be configured for providing packet transfer capabilities in accordance with the network communication protocol layers.

Accordingly, for at least the reason that the combination of Esponda and Davis do not describe muti-packet threads, the claims are patentably distinct from the references and it is requested that the rejection be withdrawn.

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Claims 2-4 and 6-18:

Claims 2-4 and 6-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Munson, Esponda as applied to claims 1 and 5 above, and further in view of Epps et al. (hereinafter Epps) U.S. 6,813,243.

Epps:

Epps describes, in the Abstract: "...A pipelined linecard architecture for receiving, modifying, switching, buffering, queuing and dequeuing packets for transmission in a communications network. The linecard has two paths: the receive path, which carries packets into the switch device from the network, and the transmit path, which carries packets from the switch to the network...."

Although Epps describes independent transmit and receive paths in a packet network, fails to overcome the inadequacies cited above in the combination of Esponda and Munson. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Although dependent claims 2-4 and 6-18 serve to add further patentable limitations to their parent independent claims, they are patentable for at least the same reasons as their parent claims, and it is respectfully requested therefore that this rejection be withdrawn.

Conclusions:

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at the number listed below so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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